AMENDMENTS

IN THE CLAIMS

Claim 1. (previously presented) A chip package structure, comprising:

a carrier having a surface with a power contact, a ground contact and a signal contact thereon, wherein the surface also has a chip bonding area, the power contact is located close to the chip bonding area, the ground contact is connected to the chip bonding area, but the signal contact is positioned further away from the chip bonding area;

a chip having an active surface and a backside such that the backside of the chip is attached to the chip bonding area of the carrier, wherein the active surface of the chip has a plurality of bonding pads thereon;

at least a passive component having at least two electrodes positioned on the carrier such that the electrodes are bonded to said power contact and said ground contact respectively;

a plurality of first conductive wires with the two ends of each conductive wire connected to one of the bonding pads of the chip and said power contact or said ground contact;

at least a second conductive wire with the two ends connected to one of the bonding pads of the chip and a corresponding signal contact such that the second conductive wire crosses over the passive component without contacting the passive component; and

an insulating material that encloses the chip, the passive component, the first conductive wires and the second conductive wire.

Claim 2. (original) The chip package structure of claim 1, wherein at least one of the first conductive wires crosses over the passive component while the remaining first conductive wires are adjacent to the passive component.

Claim 3. (previously presented) The chip package structure of claim 1, wherein the passive component is a capacitor.

Claims 4-5.**Cancelled**.

Claim 6. (previously presented) A chip package structure, comprising:

a carrier having a surface with a power ring, a ground ring and a plurality of signal contacts thereon, wherein the surface also has a chip bonding area, the power ring is located around the chip bonding area, the ground ring is connected to the chip bonding area, the signal contacts are positioned further away from the chip bonding area, the power ring has a plurality of power contacts, the ground ring has a plurality of ground contacts;

a chip having an active surface and a backside such that the backside of the chip is attached to the chip bonding area of the carrier, wherein the active surface of the chip has a plurality of bonding pads thereon;

at least a passive component having at least two electrodes positioned on the carrier such that the electrodes are bonded to one of the power contacts and one of the

ground contacts respectively;

a plurality of first conductive wires with the two ends of each conductive wire connected to one of the bonding pads of the chip and one of the power contacts or one of the ground contacts;

at least a second conductive wire with the two ends connected to one of the bonding pads of the chip and one of the signal contacts such that the second conductive wire crosses over the passive component without contacting the passive component; and

an insulating material that encloses the chip, the passive component, the first conductive wires and the second conductive wire.

Claim 7. (original) The chip package structure of claim 6, wherein at least one of the first conductive wires crosses over the passive component while the remaining first conductive wires are adjacent to the passive component.

Claim 8. (previously presented) The chip package structure of claim 6, wherein the passive component is a capacitor.

Claims 9-11. **Cancelled.**